REMARKS

This Amendment is responsive to the Office Action mailed on December 14, 2005. By this Amendment, Applicants have corrected several typographical errors in the specification, have submitted formal drawings, and have amended the claims along the lines discussed during the telephone interview. No new matter has been added. The issues raised by the Examiner in the Office Action are addressed below.

I. Objection to, and Section 112 rejection of, Claims 6 and 7

Applicants submit that the objections to Claims 6 and 7 as being of improper dependent form, and the associated rejections of these claims under Section 112, 4th paragraph, have been rendered moot by the amendments made to these claims.

II. Objection to the Drawings

As requested by the Examiner, Applicants have added the legend "Prior Art" to each of Figures 1-4.

III. Art-based rejections under Sections 102 and 103

As discussed during the interview, Applicants believe that independent Claims 1 and 8 are not anticipated by the Background of the Invention (BOI) section of the present application, and that the art-based rejections of Claims 1-11 are therefore improper.

For example, with respect to Claim 1, Applicants submit that the BOI section does not disclose "retrieving into the microprocessor a cache tag associated with the memory read request," and "within the microprocessor, comparing the cache tag to a memory address associated with the memory read request." In connection with these limitations, the prior art cache architecture shown in Figure 4 of the present application does not retrieve the cache tag into the microprocessor for a comparison, but rather uses the tag comparison circuitry of the external tag RAM to perform the comparison. Because these aspects of Claim 1 are not disclosed in the BOI section, the anticipation rejection of Claim 1 is improper.

Applicants respectfully submit that the anticipation rejection of Claim 1 is also improper because the BOI section does not disclose the following limitations of Claim 1: "subsequent to retrieving the cache tag from the cache memory bank into the microprocessor, retrieving the cache data associated with the memory read request from the cache memory bank into the

microprocessor." In this regard, in the prior art architecture of Figure 4, the cache tag and cache data elements are accessed in parallel.

With respect to independent Claim 8, the BOI section does not disclose "a bank of general purpose random access memory that stores both cache tags and cache data in separate memory locations, said general purpose random access memory lacking cache tag comparison circuitry." (Applicants submit that the addition of the limitation "lacking cache tag comparison circuitry" does not narrow Claim 8 since this limitation is inherent in the recitation of a "general purpose" random access memory.) In addition, the BOI section does not disclose the following limitations: "wherein the microprocessor is configured to retrieve a cache tag from the bank of general purpose random access memory before retrieving corresponding cache data from the bank of general purpose random access memory." Because the foregoing limitations are not disclosed by the BOI section, Applicants respectfully submit that the anticipation rejection of Claim 8 is improper.

Additional distinctions over the BOI section are recited throughout the dependent claims.

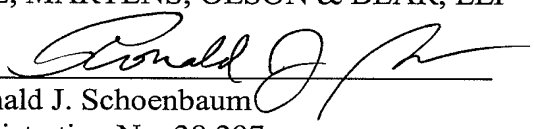
IV. Conclusion

In view of the foregoing amendments and remarks, Applicants submit that the application is now in condition for allowance. If any issues remain which can potentially be resolved by telephone, the Examiner is invited to call the undersigned attorney of record at his direct dial number listed below.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 2-2-06

By: 

Ronald J. Schoenbaum
Registration No. 38,297
Customer No. 20,995
(949) 721-2950